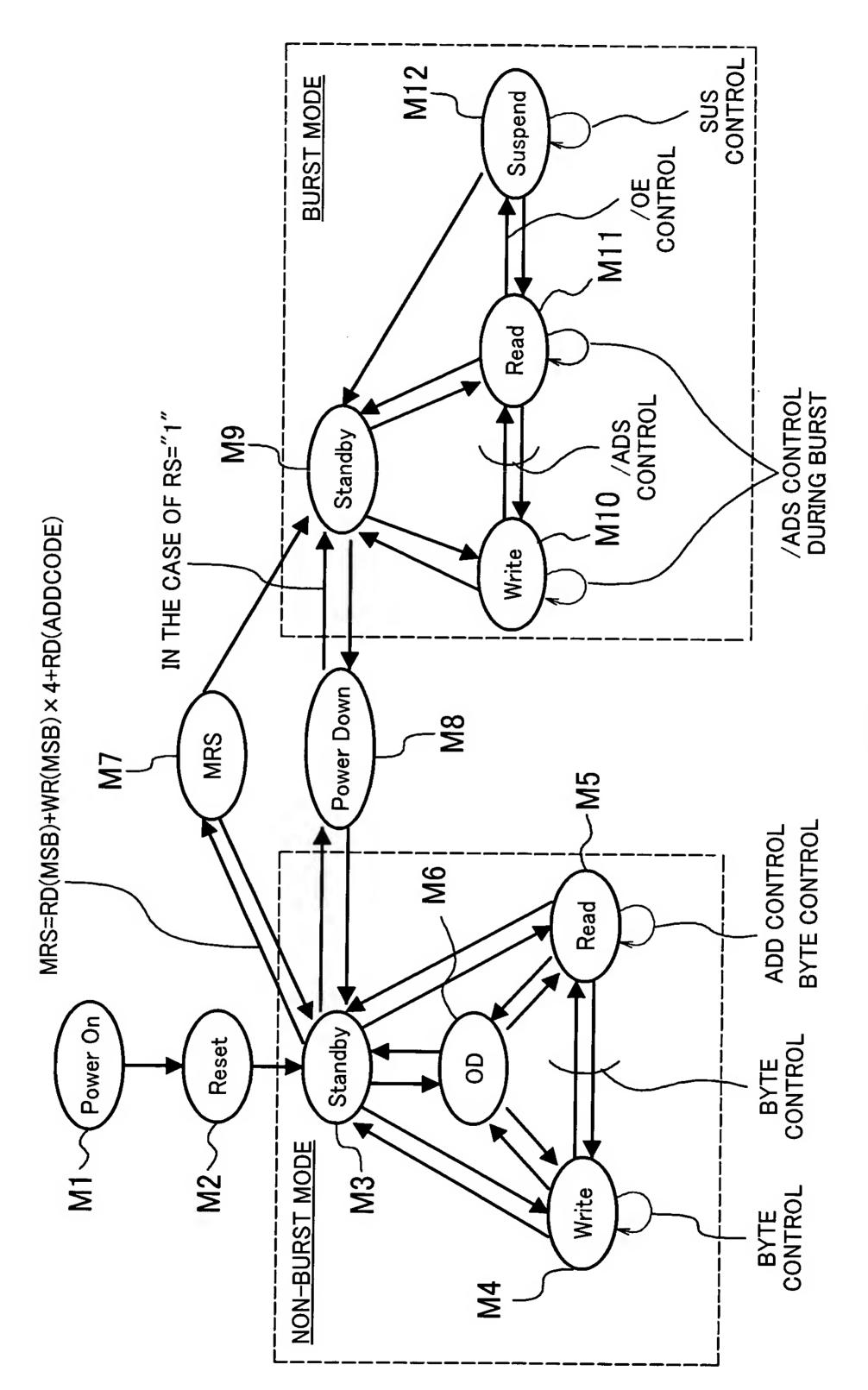
Controlling The Same
Inventor's Name: FUJIOKA, et al.

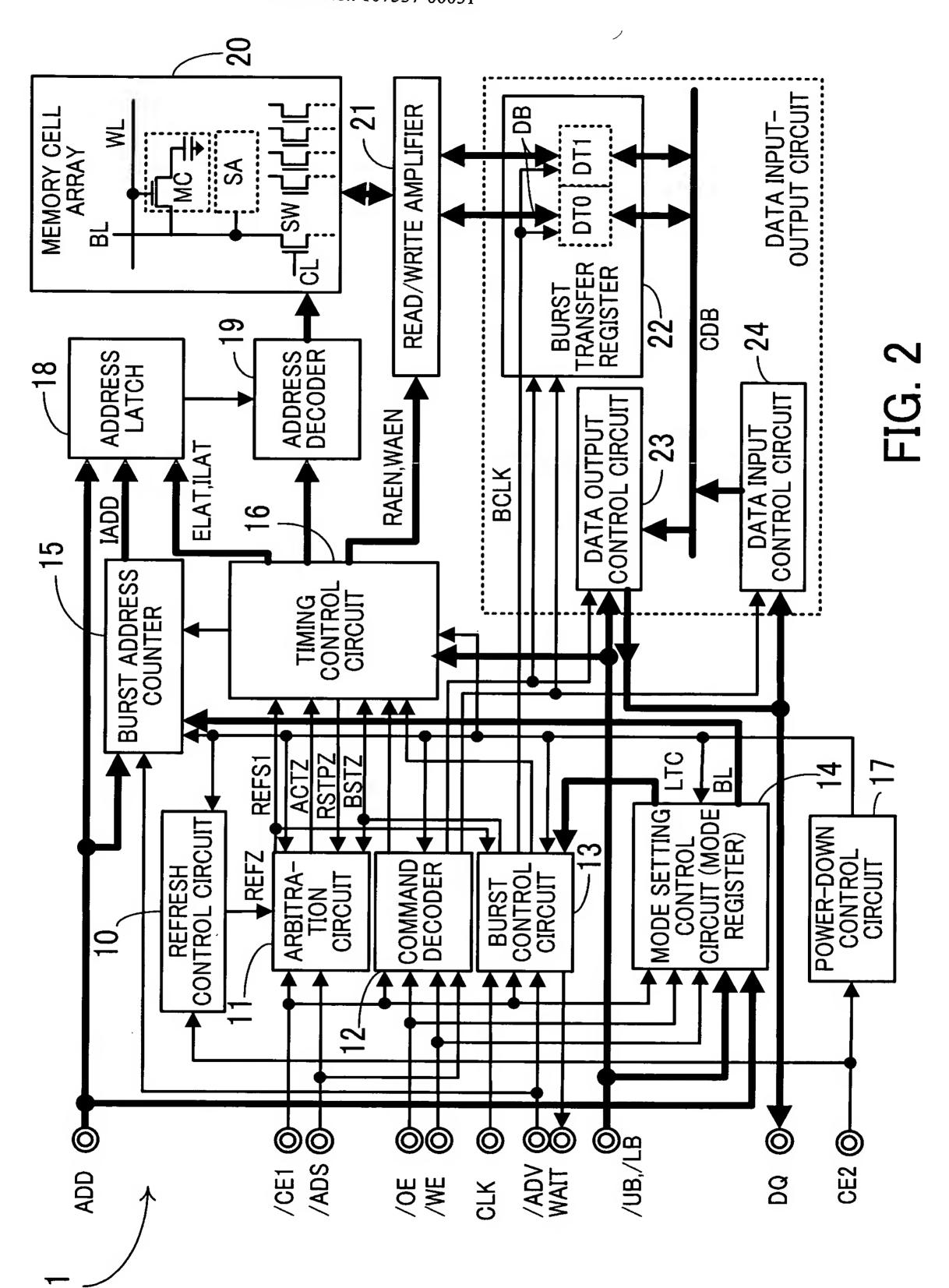
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semiconductor Method For

Controlling The Same

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FIG. 3A

	_	
12	Reset	RS
13	Count	
14	Read Latency Count	RLC
15	Read	
16	Mode	MD
11	Data Length	DL
18	Data I	Q
61	Partial Mode	M
20	Partial	PM
Add.	Func.	Sym.

FIG. 3B

Name	Description
PM	00 :16M 01 :8M 10 :Full Chip 11 :0M(Def.)
DF	00 :8word burst 01 :16word burst 10 :32word burst 11 :Continuous burst
MD	0 :Synchronous Burst Enabled 1 :Asynchronous Page Enabled(Def.)
RLC	000 :Latency Count=2 001 :Latency Count=3 010 :Latency Count=4 011 :Latency Count=5
RS	0 :Reset Enabled(Def.) 1 :Reset Disabled

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MODE	CE2	/CE1	70E	JW/	/ADS	/LB	/UB	DQ ₀₋₇	DQ ₈₋₁₅	Retention
Power Down/Reset	l 	Н	×	×	×	×	×	HiZ	Z!H	No/Partial
Standby	Н	Н	×	×	×	×	×	HiZ	Z!H	Yes
Output Disable	Ŧ	Ţ	Н	Н	×	×	×	Z!H	HiZ	Yes
Read	H	٦	Γ	Η	×	T		Dout	Dout	Yes
No Read	н	7	Γ	I	×	I	Ξ	Z!H	ZiH	Yes
Lower Byte Read	I	٦	٦	Н	×	٦	I	Dout	ZiH	Yes
Upper Byte Read	н	٦	7	Η	×	н		ZIH	Dout	Yes
Write	н	Γ	×	Τ	×	لـ ا		Din	Din	Yes
Abort Write	Н	Γ	X	Γ	×	Ξ	Ξ	Invalid	Invalid	Yes
Lower Byte Write	Н	Γ	X	Γ	×		Ι	Din	Invalid	Yes
Upper Byte Write	H	L	X	Γ	×	Ξ		Invalid	Din	Yes
Illegal	Н	٦	Γ	Γ	×	×	×		-	

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CODE 6th **MSB** 5th MSB 4th RD 5th WR MSB 3rd MSB 4th WR MSB WR MSB 2nd MSB MSB 1st MSB RD sednence CMD Add /CE1,/ADS

-1G. 5/